AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A ~~header of a nano storing~~ storage apparatus comprising:

a cantilevery array ~~including cantilevers each~~ having ~~a probe that is able to read and write information with the 'n' number of rows and the 'm' number of columns (n, m = 1, 2, 3, ...)~~ cantilever probes;

an X-redundancy cantilever array ~~to be used as a substitute~~ configured to read and write information when at least one cantilever ~~probes~~ probe of a specific row in the cantilever array ~~are~~ is defective;

a Y-redundancy cantilever array ~~to be used as a substitute~~ configured to read and write information when at least one cantilever ~~probes~~ probe of a specific column in the cantilever array ~~are~~ is defective; and

~~a header~~ a redundancy cantilever array controller ~~for controlling each part~~ configured to determine that a corresponding cantilever probe is defective when the corresponding cantilever probe is unable to read and write information, and configured to select the X-redundancy cantilever array and the Y-redundancy cantilever array when the at least one cantilever probe of the specific row and of the specific column in the cantilever array is defective.

2. (Currently Amended) The ~~header~~ apparatus of claim 1, wherein the ~~header~~ redundancy cantilever controller comprises:

~~the~~ an X-decoder ~~for receiving~~ configured to receive an X-address signal and ~~driving~~ to drive cantilevers of ~~a~~ the specific row in the cantilever array;

~~the~~ an X-redundancy decoder ~~for stopping~~ configured to stop driving ~~of~~ the X-decoder when ~~cantilevers~~ the at least one cantilever probe of ~~a~~ the specific row in the cantilever array ~~are~~ is defective and ~~selecting~~ to select the X-redundancy cantilever array;

~~the~~ a Y-decoder ~~for receiving~~ configured to receive an Y-address signal and selectively ~~driving a~~ drive the specific column in the cantilever array; and

~~the~~ a Y-redundancy decoder for ~~stopping~~ configured to stop driving ~~of~~ the Y-decoder when ~~cantilevers~~ the at least one cantilever probe of ~~a~~ the specific column in the cantilever array ~~are~~ is defective, and ~~selecting~~ to select the Y-redundancy cantilever array.

3. (Currently Amended) The ~~header~~ apparatus of claim 2, wherein the X-redundancy decoder stops driving ~~of~~ the X-decoder when the X-redundancy cantilever array is selected.

4. (Currently Amended) The ~~header~~ apparatus of claim 2, wherein the X-redundancy decoder comprises:

an output terminal ~~for outputting~~ configured to output a stop signal to the X-decoder when ~~cantilevers~~ the at least one cantilever probe of a the specific row in the cantilever array ~~are~~ is defective;

~~a unit for transferring~~ a high voltage unit configured to transfer a high voltage (V_{CC}) to the output terminal by a specific pulse signal (XRP);

~~a unit for receiving~~ a low voltage unit configured to receive the X-address signal and ~~outputting~~ to output a low voltage (0V) to the output terminal; and

a plurality of fuses connected between the output terminal and the low voltage unit ~~which outputs the low voltage,~~ and to selectively ~~defused~~ defuse when ~~cantilevers~~ the at least one cantilever probe of ~~a~~ the specific row in the cantilever array ~~are~~ is defective.

5. (Currently Amended) The ~~header~~ apparatus of claim 4, wherein the X-redundancy decoder converts signal values received from the high voltage ~~outputting~~ unit and the low voltage ~~outputting~~ unit into logical values and outputs ~~the~~ corresponding signal values to the X-decoder and the X-redundancy cantilever array.

6. (Currently Amended) The ~~header~~ apparatus of claim 4, wherein ~~as~~ the fuse~~,~~ comprises a polysilicon line or a metal line ~~is used, and the fuse~~that can be ~~melt~~ melted by using an overcurrent, cut by a laser beam or programmed by an EPROM memory cell.

7. (Currently Amended) The ~~header~~ apparatus of claim 2, wherein the ~~header~~ redundancy cantilever array controller further comprises:

a Y-switch ~~for receiving~~ configured to receive an output signal of the Y-decoder when ~~cantilevers~~ the at least one cantilever probe of a the specific column in the cantilever array ~~are~~ is defective, and ~~cutting~~ to cut off a data output of the at least one defective ~~cantilevers~~ cantilever probe of the specific column; and

a Y-redundancy switch ~~for receiving~~ configured to receive an output signal of the Y-redundancy decoder when ~~cantilevers~~ the at least one cantilever probe of ~~a~~ the specific column in the cantilever array ~~are~~ is defective, and ~~switching~~ to switch a data output of the Y-redundancy cantilever array.

8. (Currently Amended) The ~~header~~ apparatus of claim 7, wherein when the Y-redundancy cantilever array is selected, the Y-redundancy decoder stops driving ~~of~~ the Y-decoder and outputs a signal for selecting the Y-redundancy switch.

9. (Currently Amended) The ~~header~~ apparatus of claim 2, wherein the Y-redundancy decoder comprises:

an output terminal ~~for outputting~~ configured to output a stop signal to the Y-decoder when ~~cantilevers~~ the at least one cantilever probe in ~~a~~ the specific column in the cantilever array ~~are~~ is defective;

~~a unit for outputting~~ a high voltage unit configured to output a high voltage (V_{CC}) to the output terminal by a specific pulse signal (YRP);

~~a unit for receiving~~ a low voltage unit configured to receive a Y-address signal and outputting a low voltage (0V); and

a plurality of fuses connected between the output terminal and the low voltage ~~outputting~~ unit, and to selectively ~~defused~~ defuse when ~~cantilevers~~ the at least one cantilever probe of ~~a~~ the specific column in the cantilever array ~~are~~ is defective.

10. (Currently Amended) The ~~header~~ apparatus of claim 1, wherein the X-redundancy cantilever array includes ~~the~~ 'p' number of rows and ~~the~~ 'm' number of columns ($p \leq n$, $p=1, 2, 3...$), and if cantilever probes of ~~a~~ the specific row in the cantilever array having ~~the~~ an nxm number of cantilevers are defective, cantilevers of ~~a~~ the specific row of the X-redundancy cantilever array are substitutively used, and meanwhile, the Y-redundancy cantilever array includes the 'n' number of rows and 'k' number of columns ($k \leq m$, $k=1, 2, 3, ...$), and if cantilever probes of ~~a~~ the specific column in the cantilever array having the nxm number of cantilevers are defective, cantilevers of ~~a~~ the specific column in the Y-redundancy cantilever array are substitutively used.

11. (Canceled)

12. (Currently Amended) The ~~header~~ apparatus of claim ~~11~~ 2, wherein the X-decoder includes NAND gates and inverters connected to the NAND gates~~, and drives the cantilever array upon receiving the X-address signal or stops the cantilever array upon receiving a signal from the X-redundancy decoder~~.

13-15. (Canceled)

16. (Currently Amended) The ~~header~~ apparatus of claim ~~15~~ 7, wherein the Y-decoder comprises:

NAND gates ~~for receiving~~ configured to receive the Y-address signal and a signal from the Y-redundancy decoder and ~~turning~~ to turn on or off a switch of the Y-switch ~~in order to enable a data output to or stop data output from cantilevers of a specific column in the cantilever array~~; and

~~Inverters~~ inverters connected to the NAND gates.

17-18. (Canceled)